UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,083	07/17/2003	Fay Chong JR.	SUNMP234	3299

32291 7590 03/01/2006

MARTINE PENILLA & GENCARELLA, LLP
710 LAKEWAY DRIVE
SUITE 200
SUNNYVALE, CA 94085

EXAMINER	
IWASHKO, LEV	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 03/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,083	CHONG ET AL.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 8, 15, and 21-22 are rejected under U.S.C. 102(b) as being anticipated by Bennett (US Patent 5,404,464).

Claim 1. A device for addressing a shared resource, comprising:

- at least one register in communication with the shared resource, *(Abstract, lines 1-4 – State the following: "An improved bus architecture system for use in a multi-processor computer system has a shared address bus and a shared data bus, and has at least two separate memory modules." Column 8, lines 13-17 – State the following: "The clock signal for the Last Slot register is the system address bus strobe, SADDS- line 44. The initiating CPU does not issue a strobe on the SADDS- signal line 44 until it enables the address on the system address bus 16")*
- the at least one register configured to hold an address to be provided to the shared resource upon receipt of a clock signal; *(Column 8, lines 13-28 – State the following: "The clock signal for the Last Slot register is the system address bus strobe, SADDS- line 44. The initiating CPU does not issue a strobe on the SADDS- signal line 44 until it enables the address on the system address bus 16. Therefore, until the initiating CPU issues a strobe on the SADDS- signal line 44, the slot I.D. of the present request will become available on the outputs of the Slot I.D. Mapping SRAM 60, and the outputs of the Last*

Slot I.D. register 62 will represent the slot I.D. of the previous address request on the system address bus 16. The comparator 64 compares these slot I.D.s for equality. After the comparison, the slot I.D. of the new address request will be clocked into the Last Slot I.D Register 62 for the next time when the initiating processor 30 strobes the SADDS- signal line 44")

- and a multiplexer for providing a next address *(Column 6, lines 14-17 – State the following: "In the present embodiment, the MUX 56 either selects address lines A2-A13 76 or A20-A31 78 from the local address bus 70 and provides them to the slot I.D. mapping SRAM 60")*
- to the at least one register, *(Column 7, lines 28-41 – State the following: "The bandwidth maximizer circuit 38 utilizes each address while it is active on the local address bus 70. In general, each bandwidth maximizer circuit 38 stores the slot I.D. of each address request in the Last Slot I.D. register 62. Thus, after each address request, the Last Slot I.D. register 62 for each bandwidth maximizer circuit 38 contains the slot I.D. of the last address request. When a CPU module 12 initiates an address request, the initiating CPU 12 first places the address on its local address bus 70, and the bandwidth maximizer circuit 38 for that CPU 12 compares the slot I.D. for the new address with the slot I.D. of the last address. If the slot I.D. of the last request and the new request are to different slots, then the bandwidth maximizer circuit 38 for the requesting CPU issues an early address request during the period of the previous bus cycle in which the system address bus 16 is not used")*
- the multiplexer being disposed outside of a critical timing path for addressing the shared resource. *(Column 6, lines 40-44 – State the following "Accordingly, with write and read operations to addresses other than the addresses assigned to the RAM 60, the MUX 56 selects*

address lines A20-A31 78 for coupling to its outputs, and in turn to the inputs to the slot I.D. mapping SRAM 60")

Claim 8. A shared memory, comprising: *(Column 3, lines 39-49 – State the following: "The present invention is n improved bus architecture system for use in a common-bus, multi-processor system 10 with shared memory (i.e., the processors have access to common memory and shared resources). FIG. 1 illustrates a conventional multi-processor system 10 which contains a number of CPU modules 12 (i.e., CPU MODULE #1, CPU MODULE #2, ... CPU MODULE #L) and a shared memory storage area containing a number of memory modules 14 (i.e., MEMORY MODULE #1, MEMORY MODULE #2, ... MEMORY MODULE #M").*

- a data port for sending and receiving data; an address port for receiving an address to be used to locate data within the shared memory; at least one register in communication with the address port, the at least one register configured to provide the address to the address port upon receipt of a clock signal; *(Column 17, lines 5-19 – State the following: "a static random access memory with first and second data input ports and a data output port, wherein said first data input port is connected to said local address bus and said second data input port is connected to said local data bus; a storage register with an input port and an output port, said input port connected to said data output port of said static random access memory, wherein said output port of said static random access memory is divided into a first set and a second set of data bits, wherein said first set of data bits indicates the memory module which contains data that is addressed by the local address bus and wherein said second set of bits indicates if an early address request is desired;")*
- and a multiplexer for providing a next address *(Column 6, lines 14-17 – State the following: "In the present embodiment, the MUX 56 either*

selects address lines A2-A13 76 or A20-A31 78 from the local address bus 70 and provides them to the slot I.D. mapping SRAM 60")

- to the at least one register, *(Column 7, lines 28-41 – State the following: "The bandwidth maximizer circuit 38 utilizes each address while it is active on the local address bus 70. In general, each bandwidth maximizer circuit 38 stores the slot I.D. of each address request in the Last Slot I.D. register 62. Thus, after each address request, the Last Slot I.D. register 62 for each bandwidth maximizer circuit 38 contains the slot I.D. of the last address request. When a CPU module 12 initiates an address request, the initiating CPU 12 first places the address on its local address bus 70, and the bandwidth maximizer circuit 38 for that CPU 12 compares the slot I.D. for the new address with the slot I.D. of the last address. If the slot I.D. of the last request and the new request are to different slots, then the bandwidth maximizer circuit 38 for the requesting CPU issues an early address request during the period of the previous bus cycle in which the system address bus 16 is not used")*
- the multiplexer being disposed outside of a critical timing path for addressing the shared resource. *(Column 6, lines 40-44 – State the following "Accordingly, with write and read operations to addresses other than the addresses assigned to the RAM 60, the MUX 56 selects address lines A20-A31 78 for coupling to its outputs, and in turn to the inputs to the slot I.D. mapping SRAM 60")*

Claim 15. A method for addressing a shared resource, comprising:

- loading at least one register with an address to be provided to the shared resource; and providing the address to the shared resource from the at least one register upon receipt of a clock signal. *(Column 8, lines 13-28 – State the following: "The clock signal for the Last Slot register is the system address bus strobe, SADDS- line 44. The initiating CPU does not issue a strobe on the SADDS- signal line 44*

until it enables the address on the system address bus 16. Therefore, until the initiating CPU issues a strobe on the SADDS- signal line 44, the slot I.D. of the present request will become available on the outputs of the Slot I.D. Mapping SRAM 60, and the outputs of the Last Slot I.D. register 62 will represent the slot I.D. of the previous address request on the system address bus 16. The comparator 64 compares these slot I.D.s for equality. After the comparison, the slot I.D. of the new address request will be clocked into the Last Slot I.D Register 62 for the next time when the initiating processor 30 strobes the SADDS- signal line 44")

Claim 21. A method for addressing a shared resource as recited in claim 15, wherein the shared resource is a shared memory. *(Column 3, lines 39-49 – State the following: "The present invention is n improved bus architecture system for use in a common-bus, multi-processor system 10 with shared memory (i.e., the processors have access to common memory and shared resources). FIG. 1 illustrates a conventional multi-processor system 10 which contains a number of CPU modules 12 (i.e., CPU MODULE #1, CPU MODULE #2, ... CPU MODULE #L) and a shared memory storage area containing a number of memory modules 14 (i.e., MEMORY MODULE #1, MEMORY MODULE #2, ... MEMORY MODULE #M").*

Claim 22. A method for addressing a shared resource as recited in claim 15, wherein the address is provided directly to the shared resource from the at least one register upon receipt of the clock signal. *(Column 8, lines 13-28 – State the following: "The clock signal for the Last Slot register is the system address bus strobe, SADDS- line 44. The initiating CPU does not issue a strobe on the SADDS- signal line 44 until it enables the address on the system address bus 16. Therefore, until the initiating CPU issues a strobe on the SADDS- signal line 44, the slot I.D. of the present request will become available on the outputs of the Slot I.D. Mapping SRAM 60, and the outputs of the Last Slot I.D. register 62 will represent the slot I.D. of*

the previous address request on the system address bus 16. The comparator 64 compares these slot I.D.s for equality. After the comparison, the slot I.D. of the new address request will be clocked into the Last Slot I.D Register 62 for the next time when the initiating processor 30 strobes the SADDS- signal line 44")

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-4, 9-11 and 16-18 are rejected under 35 U.S.C.103(a) as being unpatentable over Bennett et al. as applied to claims 1, 8, and 15 above, further in view of Lawrence (US Patent 5,068,822), Persoon et al. (US Patent 4,627,021) and Farnsworth et al. (US Patent 4,396,915).

Bennett teaches the limitations of claims 1, 8, and 15 for the reasons above.

Bennett's invention differs from the claimed invention in that there is no specific reference to a recirculate input, an increment input, a new address input, a memory manager module, or a buffer allocator.

Bennett fails to teach claims 2-4, 9-11 and 16-18, which (more or less) respectively state the following: "A device for addressing a shared resource as recited in claim 1, wherein the multiplexer is configured to receive a recirculate input, an increment input, a new address input, and a control signal, the control signal being used to determine which of the recirculate input, the increment input, and the new address input is to be provided as the next address to the at least

one register", "A device for addressing a shared resource as recited in claim 2, wherein the new address input is provided in a time multiplexed manner to cause the at least one register to provide the address to the shared resource upon receipt of a specific clock signal", and "A device for addressing a shared resource as recited in claim 2, wherein the new address input is provided by one of a multiple input multiplexer, a memory manager module, and a buffer allocator module, each of the multiple input multiplexer, the memory manager module, and the buffer allocator module existing outside of the critical timing path for addressing the shared resource." However, Lawrence states "Referring to both FIGS. 1 and 2, each key multiplexer 20 receives as inputs: the output of the storage device 12 for the next smallest key, referred to as "bubble-up" data path; a recirculate input from the output of the associated storage device 12; the new key from input 16,; and the output from the storage device 12 for the next largest key, referred to as "readout" data path. Tag multiplexer 22 includes the same four inputs for the associated tag storage devices 14. As seen in FIG. 2, two lines 28 provide the multiplexer control signal, MUX CNTR, from control logic circuit 26 to multiplexers 20, 22" (Column 3, lines 3-13). Persoon further states: "The addresses are supplied by an address selection unit 30 which comprises an address input for receiving an address having a width of 6 bits, and an increment input having a width of 1 bit" (Column 4, lines 55-59). Farnsworth states the following: "Next, the multiplexer is addressed to read status, after which the status appearing on the first status line of the six lines (ST1-ST6) is read from BUS 7 and placed in ACCSTR. The multiplexer address will then be decremented by one and tested to see whether or not all of the status lines have been read. If not, the new multiplexer address will be input to the multiplexer to read the next status line. If all status lines (ST1-ST6) have been read, the stored status bits will be read from ACCSTR into

WRKSPS+N. If, as described above, function code bits five through seven did not signify transmit status, then the command is interpreted as transmit the contents of a designated register at DATFIL+N, determined by bits five through seven of the function code field, to retrieve the reading stored therein. This reading is then stored in WRKSPS+N. Note that in accordance with the steps shown in FIG. 23, WRKSPS+N now contains either a meter reading or status. At this time, the receive clock (RC) will be tested to determine its level. If not high, the microprocessor will wait until RC becomes high at which time it will then enable port 2 (P2) and drive the inbound transmit data line (IBTD) to "zero". Waiting for RC to go high is necessary in order to synchronize the transmission with respect to the first transmit clock (TC) following RC since, as previously described, the SCU expects an immediate receipt of message upon sending to the MTU an execute immediate transmit command" (Column 26, lines 28-57). Farnsworth further states: "This causes the SCU address buffer to thus provide the SCU address as bits SCAU00 through SCAU15 over the I/O data BUS as bits DB0 through DB7 into the microcomputer" (Column 33, lines 22-25). Farnsworth also declares a "Section Control Unit" (Column 29, lines 60), which is like a memory management unit.

It would have been obvious to one of ordinary skill in the art, having the teachings of the "Bus Control System and Method" of Bennet, the "Single Stage Extensible Sorter" of Lawrence, the "Integrated Processor" of Persoon, and Farnsworth's "Automatic Meter Reading and Control System" before him at the time the invention was made, to combine the inventions to include a recirculate input, an increment input, a new address input, a memory manager module, and a buffer allocator in order to preserve data accuracy and overall system efficiency.

5. Claims 5-7 and 12-14 are rejected under 35 U.S.C.103(a) as being unpatentable over Bennett et al. as applied to claims 1 and 8 above, further in view of Ruetz (US Patent 5,005,120).

Bennett teaches the limitations of claims 1 and 8 for the reasons above.

Bennett's invention differs from the claimed invention in that there is no specific reference to a register chain.

Bennett fails to teach claims 5-7 and 12-14, which (more or less) respectively state the following: "A device for addressing a shared resource as recited in claim 1, wherein the at least one register includes a register chain, the register chain being defined by a number of registers connected in a serial manner, the number of registers including a first register and a last register, the first register being provided with the next address from the multiplexer", "A device for addressing a shared resource as recited in claim 5, wherein each of the number of registers has an input and an output, the output of each register that is not the last register in the register chain being connected to the input of a sequential register in the register chain to define the serial manner of connection, the output of the last register in the register chain being connected to an input of the multiplexer", and "A device for addressing a shared resource as recited in claim 5, wherein each of a number of portions of the shared resource is provided with one of a number of addresses from the output of the number of registers in the register chain upon receipt of the clock signal." However, Ruetz states:"The registers P.sub.k1, P.sub.k2, . . . , P.sub.kn.sbsb.k each have an input terminal to receive an input signal from x.sub.1 or from the multiplexer MUXk or from the preceding register in the sequence" (Column 8, lines 57-63). Ruetz further states: "The goals of the invention may be realized in another embodiment by providing an array of two or more rows of shift registers (or simple sub-processors), with each row of registers

being connected together serially end-to-end, with each row of registers receiving an externally generated input signal, and with each row of registers feeding a signal processor, where an output signal from a first row of registers is routed to a multiplexer or similar programmable means that also receives an externally-generated signal and an output signal of this multiplexer is fed to a second row of processors" (Column 2, lines 34-45). Finally, Ruetz states: "The n-bit content of each register in row k (1<k<N) may also be deposited on a collective line L.sub.k at each clock cycle for delivery to the processor P, as shown in FIG. 8. The collective line L.sub.k may be a collection of n.multidot.n.sub.k parallel lines, with each of these parallel lines carrying information on the current value of one bit in one of the registers P.sub.kj (1<j<n.sub.k)" (Column 3, lines 36-43).

It would have been obvious to one of ordinary skill in the art, having the teachings of the "Bus Control System and Method" of Bennet, and Ruetz's "Compensating Time Delay" before him at the time the invention was made, to combine the inventions to include a register chain so that data would be more accurately referenced and found, making the entire system more efficient.

6. Claims 19-20 are rejected under 35 U.S.C.103(a) as being unpatentable over Bennett et al. as applied to claim 15 above, further in view of Ruetz (US Patent 5,005,120).

Bennett teaches the limitations of claim 15 for the reasons above.

Bennett's invention differs from the claimed invention in that there is no specific reference to a register chain.

Bennett fails to teach claims 19-20, which respectively state the following: "A method for addressing a shared resource as recited in claim 15, further comprising: providing a register

chain defined by the at least one register and a number of additional registers; loading the number of additional registers with a number of additional addresses to be provided to the shared resource; and providing each of the number of additional addresses to different portions of the shared resource from the number of additional registers upon receipt of the clock signal used to provide the address to the shared resource from the at least one register" and "A method for addressing a shared resource as recited in claim 19, further comprising: shifting the address and the number of additional addresses through the register chain to allow each of the address and the number of additional addresses to be provided to appropriate portions of the shared resource at a specific clock cycle." However, Ruetz states:"The registers P.sub.k1, P.sub.k2, . . . , P.sub.kn.sbsb.k each have an input terminal to receive an input signal from x.sub.1 or from the multiplexer MUXk or from the preceding register in the sequence" (Column 8, lines 57-63). Ruetz further states: "The goals of the invention may be realized in another embodiment by providing an array of two or more rows of shift registers (or simple sub-processors), with each row of registers being connected together serially end-to-end, with each row of registers receiving an externally generated input signal, and with each row of registers feeding a signal processor, where an output signal from a first row of registers is routed to a multiplexer or similar programmable means that also receives an externally-generated signal and an output signal of this multiplexer is fed to a second row of processors" (Column 2, lines 34-45). Finally, Ruetz states: "The n-bit content of each register in row k (1<k<N) may also be deposited on a collective line L.sub.k at each clock cycle for delivery to the processor P, as shown in FIG. 8. The collective line L.sub.k may be a collection of n.multidot.n.sub.k parallel lines, with each of

these parallel lines carrying information on the current value of one bit in one of the registers P.sub.kj (1<j<n.sub.k)" (Column 3, lines 36-43).

It would have been obvious to one of ordinary skill in the art, having the teachings of the "Bus Control System and Method" of Bennet, and Ruetz's "Compensating Time Delay" before him at the time the invention was made, to combine the inventions to include a register chain so that data would be more accurately referenced and found, making the entire system more efficient.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lev Iwashko

MATTHEW D. ANDERSON
PRIMARY EXAMINER